WEST Search History

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DATE: Thursday, October 20, 2005

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L14	L13 and (execut$4 near5 (sequen$4 or order$4))	14
☐	L13	l1 with L12	157
☐	L12	(first adj (memory or storage or buffer or queue)) with (second adj (buffer or memory or storage or queue))	45985
☐	L11	l1 same L10	331
☐	L10	(first adj (memory or storage or buffer or queue)) same (second adj (buffer or memory or storage or queue))	55533
☐	L9	L7 and (execut$4 near5 (sequen$4 or order$4))	80
☐	L8	L7 same (execut$4 near5 (sequen$4 or order$4))	2
☐	L7	l1 same L5	637
☐	L6	l1 and L5	3679
☐	L5	(first near2 (memory or storage or buffer or queue)) same (second near2 (buffer or memory or storage or queue))	99710
☐	L4	L3 same (sequen$4 or order$4)	44
☐	L3	L1 same dual	272
☐	L2	L1 same (first with second)	1864
☐	L1	((single or one) near2 (memory or storage or buffer or queue) near2 control$4)	12628

END OF SEARCH HISTORY

L14: Entry 9 of 14 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6373598 B1
TITLE: Facsimile machine for use in combination with PC

Detailed Description Text (4):
Referring back to FIG. 2, the facsimile machine 1 Includes a central processing unit (CPU) 10 which is connected to various components to be described later with signal bus lines. The CPU 10 controls its associated components in accordance with a predetermined communication control sequence and executes data communication, that is, facsimile transmission and reception.

CLAIMS:

13. A facsimile system comprising:

a facsimile machine having a facsimile body housing an input/output interface, and a first storage device; and

a personal computer connected to said facsimile machine through said input/output interface of said facsimile machine, said personal computer having a computer body, separate from said facsimile body, that houses a data storage device acting as a second storage device for the facsimile machine, wherein

said facsimile machine further includes control means for controlling a selected one of said first storage device and said second storage device to store facsimile transaction information, said control means also being housed in said facsimile body, said control means controlling said second storage device of the personal computer to store the facsimile transaction information when said control means detects that said facsimile machine and said personal computer are connected to each other, and said control means controls said first storage device of the facsimile machine to store the facsimile transaction information when said control means detects that said facsimile machine and said personal computer are not connected to each other.

L14: Entry 1 of 14 File: PGPB May 12, 2005

DOCUMENT-IDENTIFIER: US 20050102479 A1
TITLE: Storage system, and method for controlling the same

Detail Description Paragraph:
[0071] When a disk array apparatus is the one equipped with a very ordinary interface as the connection interface with the host computer 5, like the switching device 201 as described above, the disk array apparatus can be used as the second storage controller 20 of the embodiment and, for example, in a storage system using a disk array apparatus having a higher performance as the first storage controller 10 and a disk array apparatus having a lower performance than the other one as the second storage controller 20, a merit can be produced that the functions of the first storage controller 10 can be applied to the second storage controller 20.

Detail Description Paragraph:
[0083] Next, the priority control function included in the first storage controller 10 will be described. The first storage controller 10 stores the priority management table shown in FIG. 9. In the priority management table, the relations of Destination_ID, Source_ID and the delay time are described. The delay time is used as, for example, a parameter for determining the starting time of execution of a process that may increase the load of processing of the microprocessor 121. The priority control function is a function that controls the order of execution of the data input and output corresponding to the data frame received by the first storage controller 10 from the host computer 5, according to the delay time set in the priority management table. The contents of the priority management table may be registered automatically by a function of the first storage controller 10 or may be registered in a manual operation by an operator.

Detail Description Paragraph:
[0086] If a delay time is set in (S1015), the first storage controller 10 checks whether another data frame B exists waiting to be processed in a queue managed by the control memory 123 in the storage device control unit 12 (S1020) and, if the data frame B exists waiting, causes the starting of execution of the process for data frame A stand by for the period of the delay time set in the priority management table corresponding to the contents of the data frame A (S1021). The starting time of which processes for the data frame should be delayed is adequately determined taking into consideration the load of processing imposed on the microprocessor 121 such that the data input/output process will be executed in an adequate order according to the needs of users. Arrangement may be such that the control of the order of executing processes using the delay time as a parameter can be determined automatically by the storage system or that the control of the order can be set by a user from a control terminal connected to the storage system. After the delay time has passed, the first storage controller 10 executes data input and output for data frame A (S1022) and transmits to the host computer 5 a data frame in which the report of completion is described (S1023).

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L14: Entry 3 of 14 File: PGPB Mar 13, 2003

DOCUMENT-IDENTIFIER: US 20030048677 A1
TITLE: Semiconductor device having a dual bus, dual bus system, shared memory dual bus system, and electronic instrument using the same

Summary of Invention Paragraph:
[0018] In the one aspect of the invention, the memory controller may give processing priority to a first memory access request inputted through the high-speed bus when the first memory access request competes with a second memory access request inputted through the low-speed bus.

Detail Description Paragraph:
[0076] According to the priority processing criterion stored in the register 102 of FIG. 3, a memory access request inputted through the high-speed bus 40 is first selected in step 8 of FIG. 4, and the memory access request A is executed as the first priority order as noted above.

Detail Description Paragraph:
[0080] In the step 10 of FIG. 4, because the answer to "Has Memory Access Request Inputted through High-speed Bus 40 been executed twice in succession?." is YES, the memory access request D through the low-speed bus 40 is executed as the third priority order in step 11.

Detail Description Paragraph:
[0085] In the following step 9, because there remains only the memory access requests E inputted through the low-speed bus 40, the memory access request E in step 12 is executed as the sixth priority order. In the next step 13, determination is made that there are no remaining memory access requests, and the process returns to step 1 to wait for the next memory access request.

Detail Description Paragraph:
[0086] In this manner, the order of execution is A, B, D, C. A2 and B.

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L14: Entry 4 of 14 File: PGPB Feb 13, 2003

DOCUMENT-IDENTIFIER: US 20030030644 A1
TITLE: System for testing multiple devices on a single system and method thereof

Detail Description Paragraph:
[0033] Requests from the same client can also be routed to different memory controllers, allowing the client to access memory address blocks spanning multiple memory modules. For some clients, it is important that read data be returned in the same order that it was requested. In one embodiment, an interlocking method is used to preserve the order that requests originating from the same client are serviced by the two memory controllers. In step 290, an interlock monitors the activity of each client. When a request arrives and is routed to one memory controller, the second memory controller is prohibited from accepting subsequent requests until the first memory controller has finished. Note that each memory controller represents a pipeline that may contain several requests in various stages of completion.

CLAIMS:

5. The method as in claim 1, wherein data access requests routed to the plurality of memory controllers are executed by the plurality of memory controllers in the order in which the data access requests are received.

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L14: Entry 5 of 14 File: USPT Apr 5, 2005

DOCUMENT-IDENTIFIER: US 6877044 B2
TITLE: Distributed storage management platform architecture

Detailed Description Text (357):
Commands received by a target driver with ordered queue tags can present some issues. While it may be sufficient that any command sent by an initiator driver, which is the result of a command received with an ordered tag, is given an ordered tag, and that this is sufficient to guarantee correct order of execution, this does not guarantee that status is delivered to the host in the correct order.

CLAIMS:

26. The apparatus of claim 24, wherein a first storage-side multi-port controller is communicatively coupled to a second storage-side multi-port controller, wherein a first one of said SVEs comprises said first storage-side multi-port controller, a second one of said SVEs comprises said second storage-side multi-port controller, and said first and said second storage-side multi-port controllers are ones of said storage-side multi-port controllers.

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L14: Entry 6 of 14 File: USPT May 13, 2003

DOCUMENT-IDENTIFIER: US 6564291 B1
TITLE: Multi-function peripheral storage device buffer system

Detailed Description Text (7):
It will be noted that the SRAM 56, ROM 58, and the external instruction memory 64 may together comprise the internal memory 32 of FIG. 1. It will be further noted that the processor 52 may load executable instructions from one or both of the memory devices 58 and 64 into the SRAM 56 for execution therefrom, for example, in order to reduce instruction fetching time.

CLAIMS:

1. A peripheral storage device buffer system, comprising: a first memory device; a control circuit in electrical communication with the first memory device, a processor associated with the peripheral storage device, and a buffer manager associated with the peripheral storage device, the control circuit having a control state associated therewith; wherein the control circuit is adapted to selectively provide electrical communication between the first memory device and one of the processor and the buffer manager according to the control state, and wherein the control circuit is in electrical communication with a second memory device associated with the peripheral storage device, and wherein the control circuit is adapted to selectively provide electrical communication between the first memory device and one of the processor and the buffer manager, and to selectively provide electrical communication between the second memory device and the other of the processor and the buffer manager according to the control state.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	23693970	@ad<"20030317"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:17
L9	937	((first adj2 clock) with writ$4) same ((second adj2 clock) with read$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:17
L10	328	L9 same (frequenc$3 rate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:17
L11	110	L10 same synchron$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:17
L12	99	L11 and L8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:18
S1	21	US-4903146-$.DID. OR US-5051839-$.DID. OR US-5172244-$.DID. OR US-5184184-$.DID. OR US-5341196-$.DID. OR US-5434650-$.DID. OR US-5485246-$.DID. OR US-5510876-$.DID. OR US-5546164-$.DID. OR US-5583615-$.DID. OR US-5694201-$.DID. OR US-5784663-$.DID. OR US-5812900-$.DID. OR US-5897236-$.DID.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/17 12:54
S2	1	2001-135009	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/17 12:54
S3	26	"135009"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/17 12:54
S4	2	"0135009".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/17 12:54
S5	479	"communications interface" same register same stor$4 same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 12:57
S6	96	S5 and "control circuit"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 15:26
S7	60	S6 and (chronological "in order")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:14

S8	1323	((reduc$3 decreas$3 diminish$3 cut$4 shrink$3 lower$3) with power with (consumption use utiliz$5)) same ((disk disc) near2 drive)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 13:22
S9	99	S8 and (communicat$4 near3 interfac$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 13:23
S10	47	S9 and register and memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 15:20
S11	12025	task near2 (management schedul$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 15:21
S12	244	S11 same register same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 15:22
S13	73	S12 same (associat$3 connect$3 correlat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 15:49
S14	23692626	@ad<"20030317"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 15:50
S15	59	S13 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 16:09
S16	19	S13 same access$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 16:09
S17	14	S16 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/17 16:10
S18	18	("4249248" "5717946" "6819334" "20020033971" "20030187569" "20040133718" "20040228166" "20050114575" "20020199048").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 10:48
S19	2	"6338110".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 10:48
S20	69658	(register memory buffer queue storage) with (stor$4 near2 (data information)) with transfer$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:16

S21	99481	(first near2 (memory buffer queue storage)) same (second near2 (memory buffer storage queue))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:27
S22	606493	control$4 near5 (writ$4 stor$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:51
S23	9538	S20 and S21 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 11:20
S24	1258	S20 same S21 same S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 11:20
S25	23693949	@ad<"20030317"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:22
S26	854	S24 and S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 11:23
S27	119	S24 same interfac$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 11:23
S28	98	S27 and S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:46
S29	13681	((first near2 (memory buffer queue storage)) with address$2) same (second near2 (memory buffer storage queue))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:28
S30	279	S20 same S29 same S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 11:29
S31	22	S30 same interfac$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:14
S32	24582	register near4 (data information) near4 transfer$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:16
S33	10548	(first adj2 memory) near5 address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:17

S34	2506	(second adj2 memory) with (data information) with associat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:18
S35	226579	control$4 with writ$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:19
S36	3	S32 same S33 same S34 same S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 14:21
S37	5	S32 same S33 same S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 13:22
S38	479	"communications interface" same register same stor$4 same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 15:27
S39	378	S38 same control$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 15:27
S40	40	S39 same first same second	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 15:40
S41	23	S39 same fifo	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/18 15:40
S42	42043	(register memory buffer queue storage) near5 stor$4 near3 (data information) near6 transfer$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:48
S43	253252	((register memory buffer queue storage) near5 (address location)) near5 (register memory buffer queue storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:49
S44	1232252	((register memory buffer queue storage) near5 (writ$4 stor$4)) near5 (register memory buffer queue storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:50
S45	255288	control$4 near5 (writ$4 stor$4) near5 (data information)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:51
S46	1307	S42 same S43 same S44 same S45	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:52

S47	112	S46 same host	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 15:52
S48	90	S47 and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 16:08
S49	4	"6799242".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/18 16:08
S50	99	("5943613" "4599745" "5452420" "5649210" "5815567" "5936990" "5943623" "6073179" "6088385" "6111936" "6128564" "6154524" "4952817" "5396636" "5585792" "5862393" "5668553" "5739597" "5909586" "5943404" "4567557" "4587497" "4905237" "5293639" "5450073" "5486830" "5490134" "5504864" "5764693" "5931950" "5983362" "6026288" "6049702" "6211701" "6223045" "6211701" "6223045" "4311986" "4313223" "4317175" "4437046" "4514855" "4574355" "4884287" "4945297" H000850 "4972440" "4996453" "5017799" "5193107").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 14:01
S51	8	fifo with ((specific exact precise) adj number) with ((data information) near5 (writ$4 stor$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 14:03
S52	9	(fifo "first in first out" "first-in first-out") with ((specific exact precise) adj number) with ((data information) near5 (writ$4 stor$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 18:16
S53	1536	(first adj2 clock) same (second adj2 clock) same writ$4 same read$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 18:18
S54	2382	((first adj2 clock) with (writ$4 read$4)) same ((second adj2 clock) with (writ$4 read$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 18:19
S55	936	((first adj2 clock) with writ$4) same ((second adj2 clock) with read$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 18:19
S56	328	S55 same (frequenc$3 rate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/19 18:20
S57	110	S56 same synchron$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/20 08:17